



Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(✓) Final Specifications

Module	14.0"(13.97") HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	BI40XTN07.5
H/W	0A
Note ()	<i>LED Backlight with driving circuit design</i>

Customer

Date

Checked &
Approved by

Date

Note: This Specification is subject to change
without notice.

Approved by

Date

Buffy Chen**08/26/2020**

Prepared by

Date

Viki Li08/26/2020

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
I.0 2020/08/26	All	First Edition for Customer		



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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2. General Description

BI40XTN07.5 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

BI40XTN07.5 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95			
Active Area	[mm]	309.399 x 173.952			
Pixels H x V		1366 x 3(RGB) x 768			
Pixel Pitch	[mm]	0.2265 x 0.2265			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White(TN)			
White Luminance (ILED=18 mA) (Note: I _{LED} is LED current)	[cd/m ²]	250 typ. (5 points average) 213 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.4W max. (Include Logic and Blu power)			
Weight	[Grams]	285 max.			
Physical Size With PCB	[mm]		Min.	Typ.	Max.
		Length	315.51	315.81	316.11
		Width	185.77	186.07	186.37
		Thickness	-	-	3.0 W/O FPC 5.0 W/ FPC
Electrical Interface		1 Lane eDP1.2			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		262K colors (RGB 6-bit)			
Temperature Range					
Operating	[°C]	0 to +50			
Storage (Non-Operating)	[°C]	-20 to +60			
RoHS Compliance		RoHS Compliance			



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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

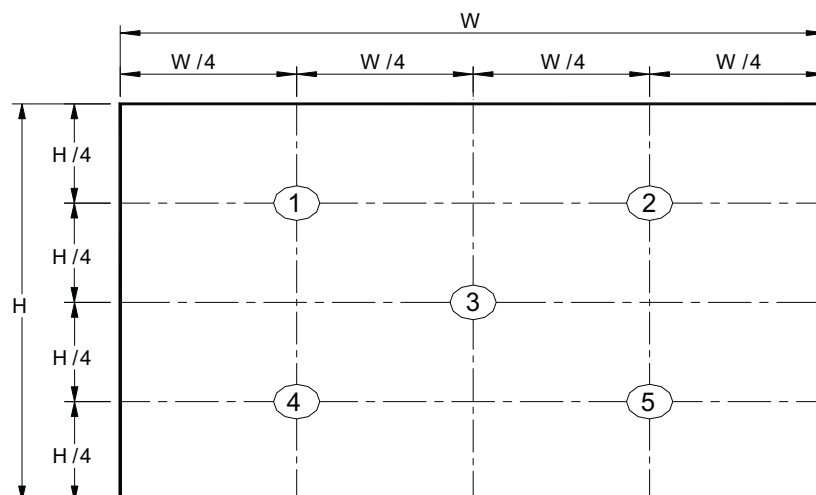
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance $I_{LED}=18mA$		5 points average	213	250	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right)	40	45	-	degree	4, 9
	θ_L	CR = 10 (Left)	40	45	-		
	ψ_H	Vertical (Upper)	10	15	-		
	ψ_L	CR = 10 (Lower)	30	35	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		300	400	-		4, 6
Cross talk	%		-	-	4		4, 7
Response Time	T_{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coordinate	Red	R _x	0.532	0.562	0.592	-	4
		R _y	0.306	0.336	0.366		
	Green	G _x	0.314	0.344	0.374		
		G _y	0.544	0.574	0.604		
	Blue	B _x	0.133	0.163	0.193		
		B _y	0.096	0.126	0.156		
	White	W _x	0.283	0.313	0.343		
		W _y	0.299	0.329	0.359		
			-	45	-		
NTSC	%		-	45	-		



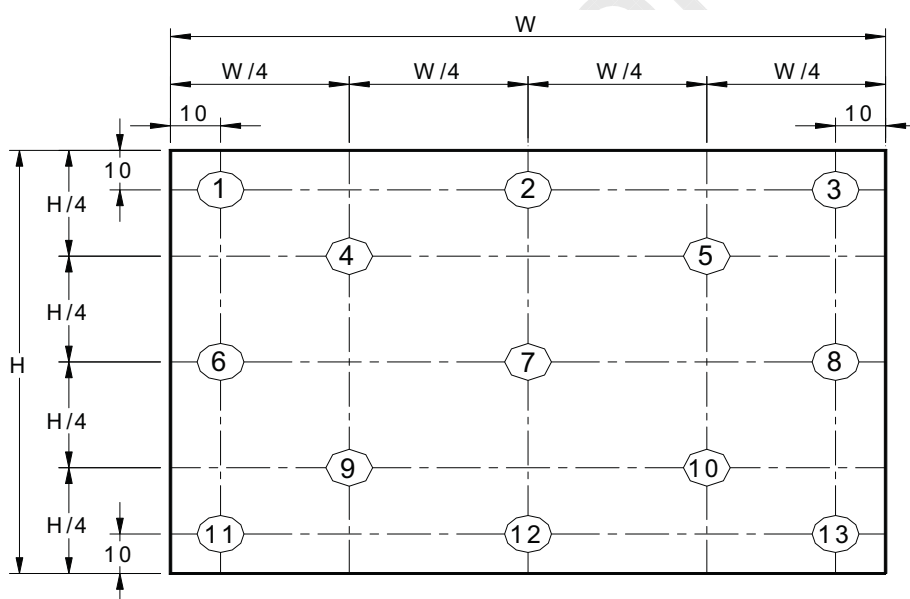
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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

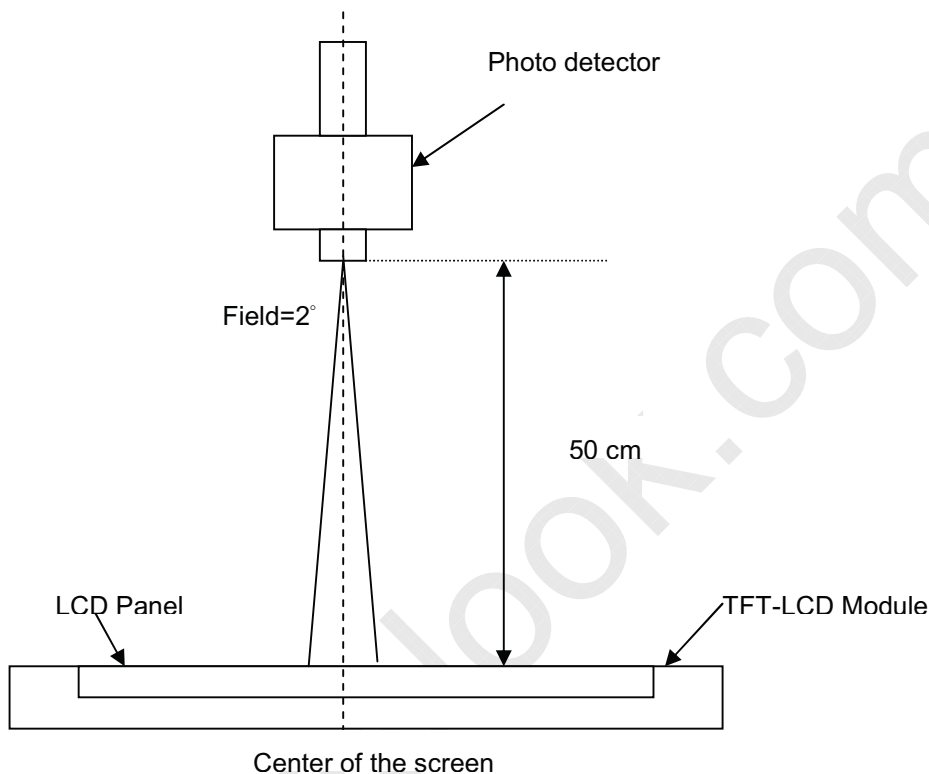


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Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$



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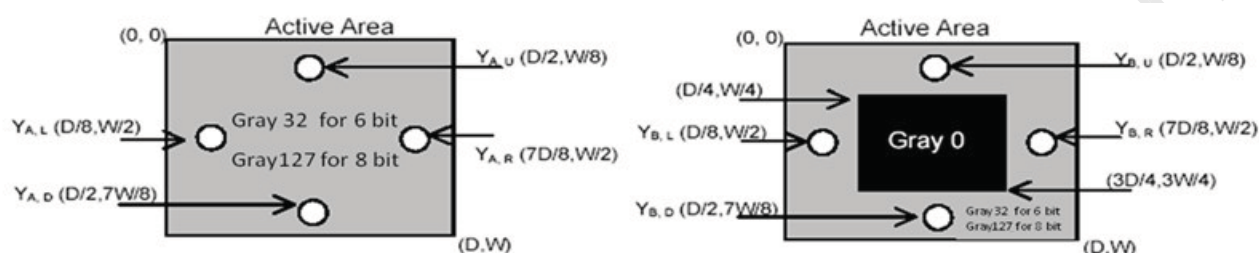
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

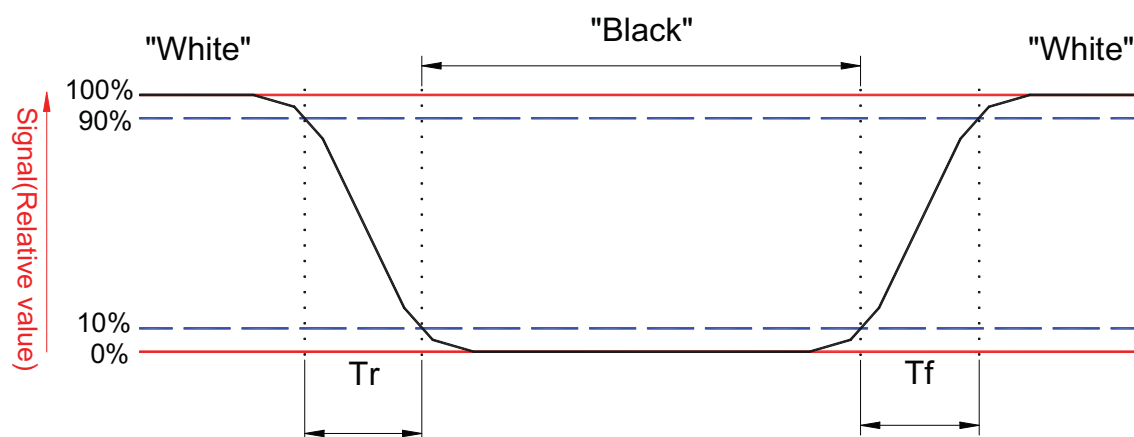
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



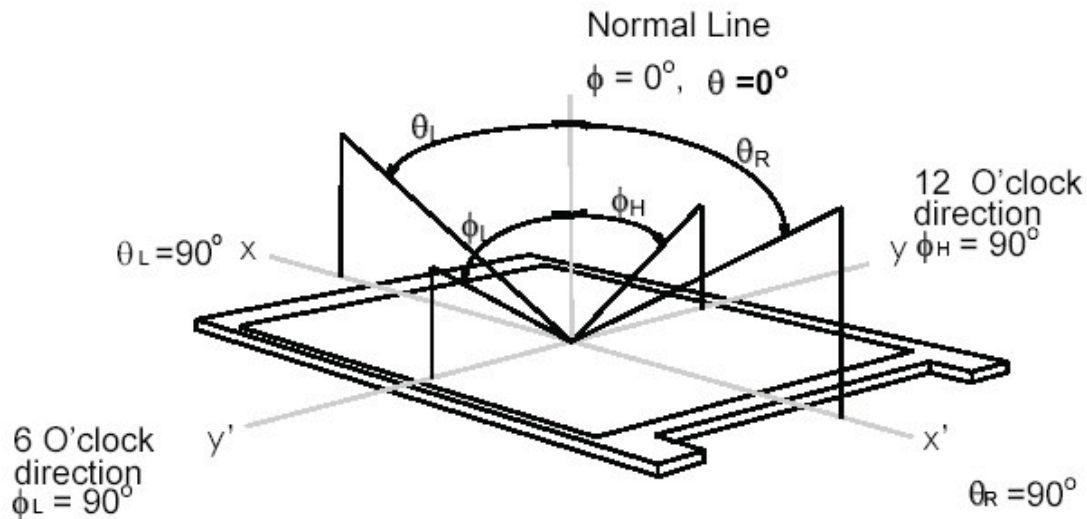


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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



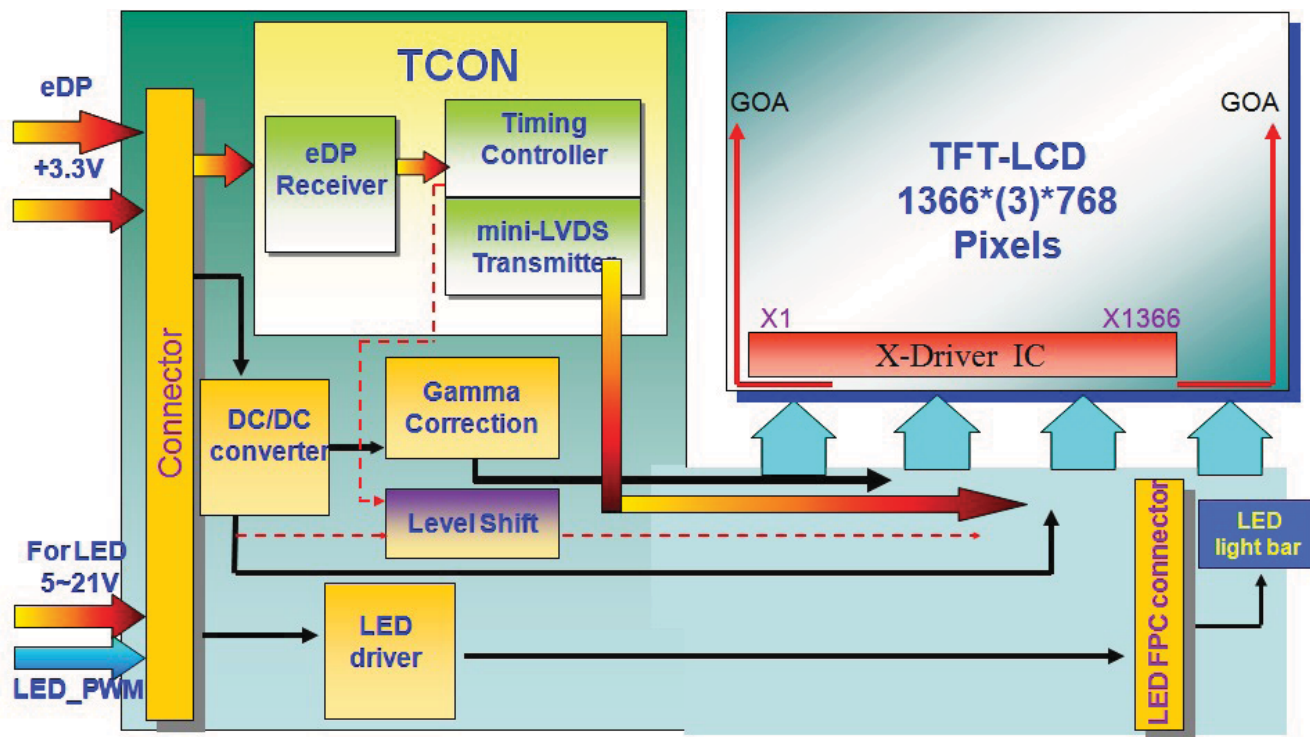


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3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin one channel Module





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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operating Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

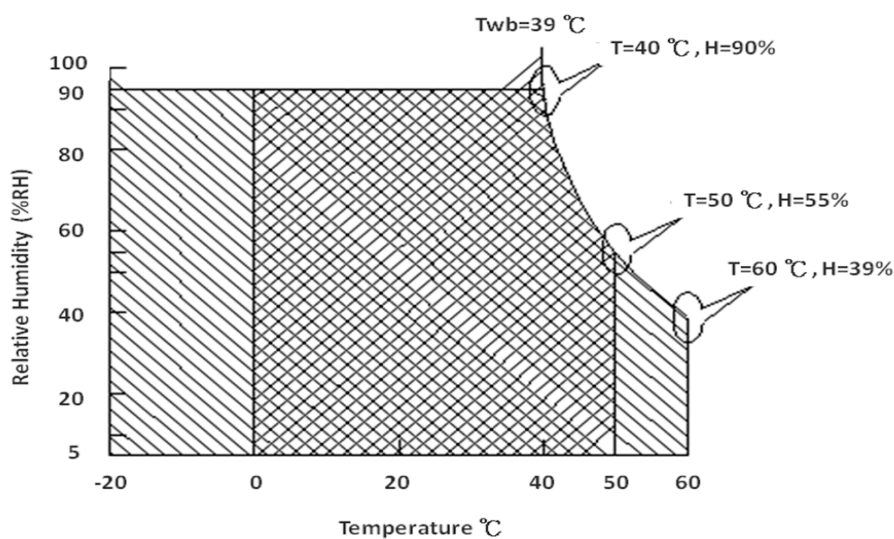
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

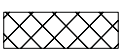
Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



Operating Range 

Storage Range  + 



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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

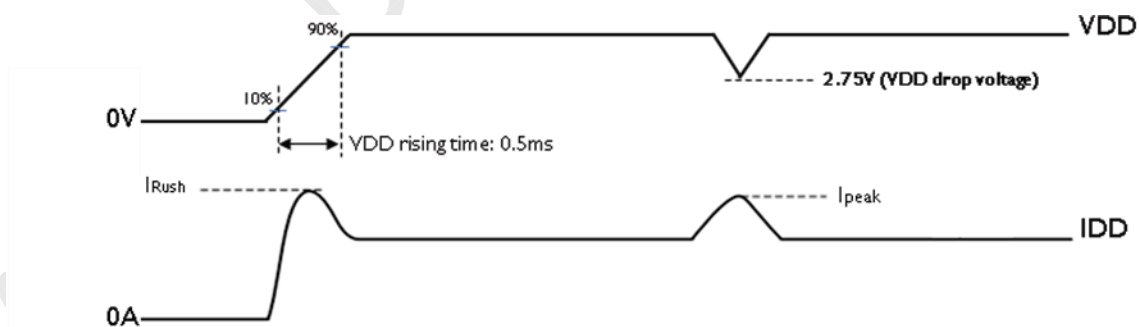
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.7	0.8	[Watt]	Note 1
IDD	IDD Current	-		267	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
Ipeak	Peak Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

$$IDD(Max)=PDD(Max) / VDD(Min)$$

Note 2 :

- IRush: VDD measured rising timing @ 0.5ms
- IPeak: VDD drop Voltage $\geq 2.75V$ at this Ipeak current

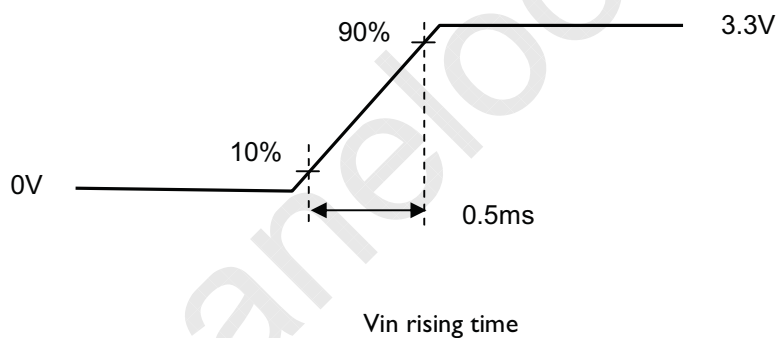
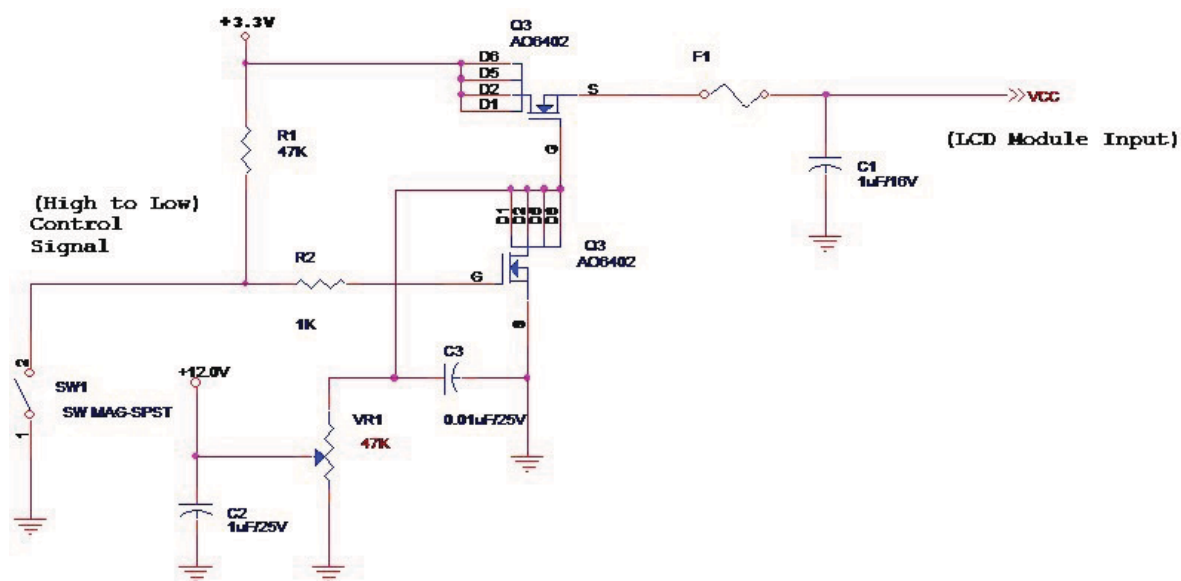




c. IRush Measure Condition:

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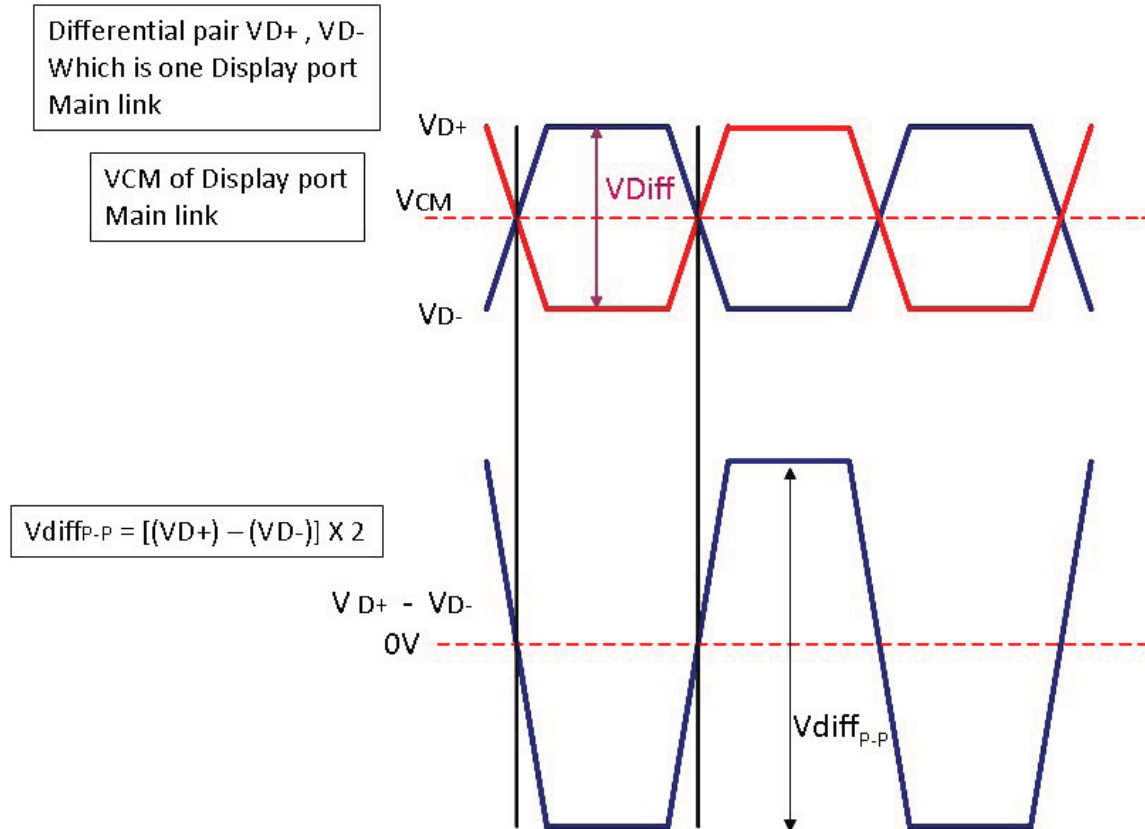
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5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Fallow as VESA display port standard

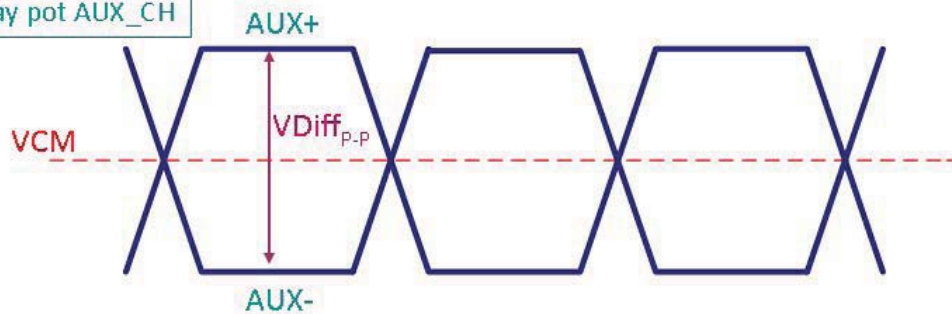


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Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{p-p}	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Fallow as VESA display port standard

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard



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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.7	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=18 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.6	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.0	[Volt]	
PWM Logic Input Low Level		-	-	0.6	[Volt]	
PWM Input Frequency	FPWM	200	-	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm



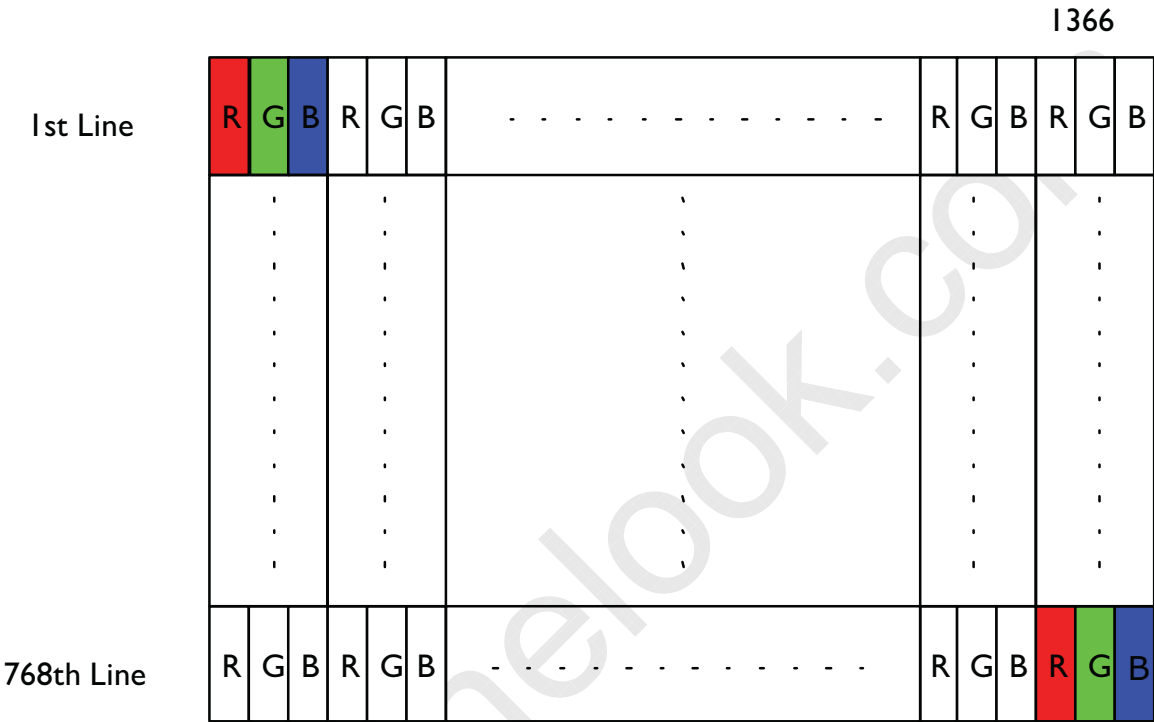
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6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





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6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	MSAK24025P30 or compatible
Mating Housing/Part Number	IPEX-20453 or compatible



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6.2.2 Pin Assignment (I Lane)

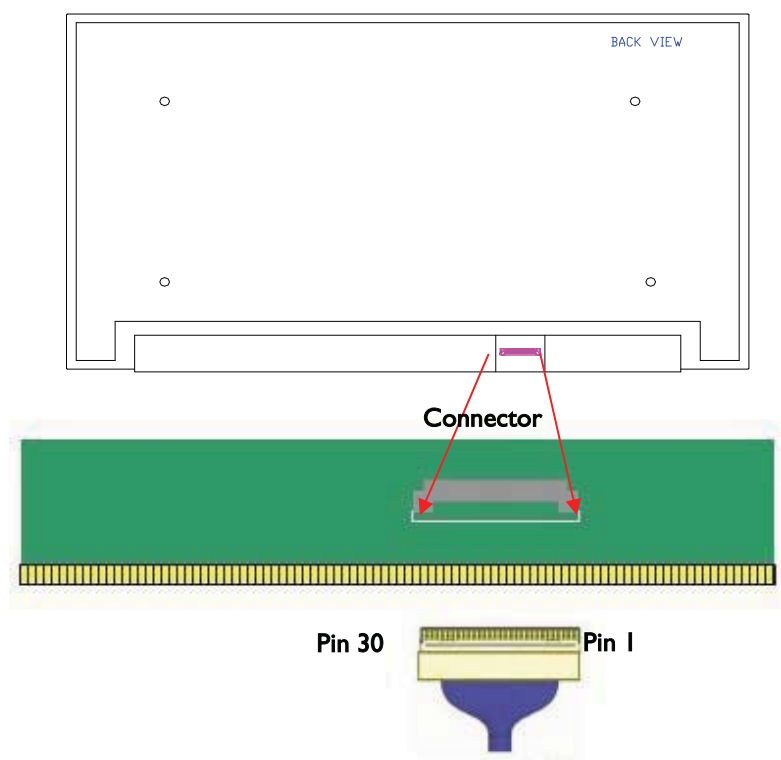
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect (Reserved for DCR)
2	H_GND	High Speed Ground
3	LaneI_N	Complement Signal Link Lane I
4	LaneI_P	True Signal Link Lane I
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable (Optional)
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	H_SYNC or NC	H_SYNC function(Optional) or NC
25	NC	No connect (Reverse for AUO TEST only)
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect (Reserved for CM)



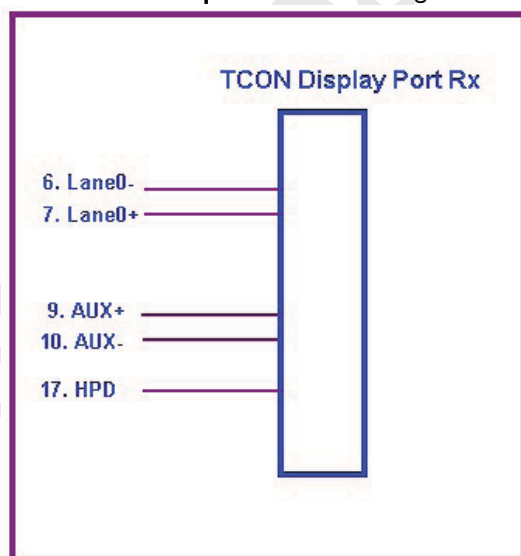
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Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.





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6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the I366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		I/ T _{Clock}	68.6	76.3	80	MHz
Vertical Section	Period	T _V	780	798	768+A	T _{Line}
	Active	T _{VD}	768			
	Blanking	T _{VB}	12	30	A	
Horizontal Section	Period	T _H	1466	1592	1366+B	T _{Clock}
	Active	T _{HD}	1366			
	Blanking	T _{HB}	100	226	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = $(1366+B)*(768+A)*60 < 80\text{MHz}$

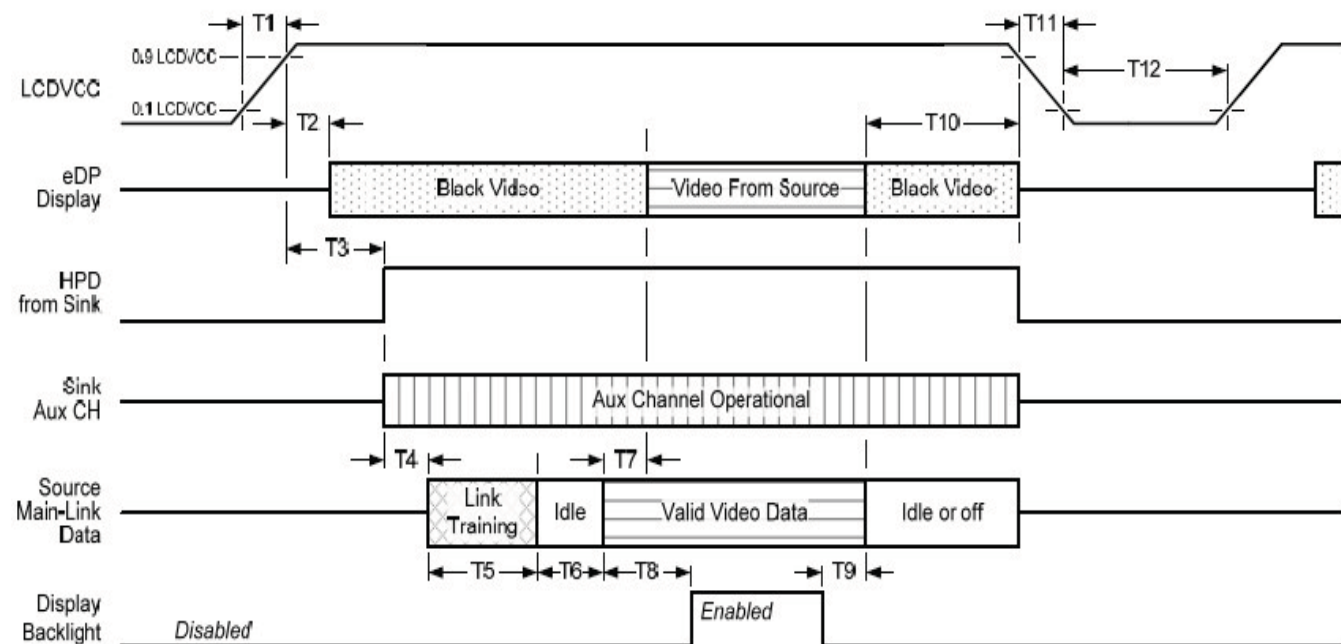


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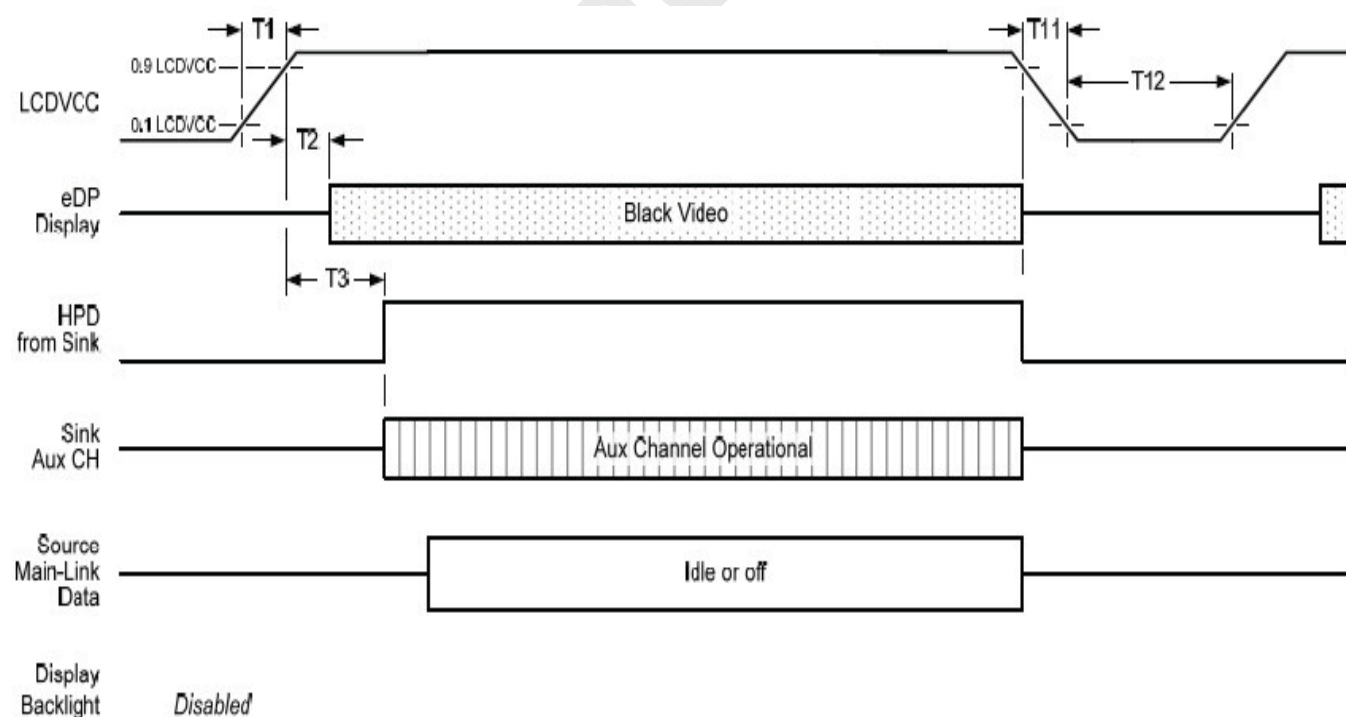
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only



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Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (within T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

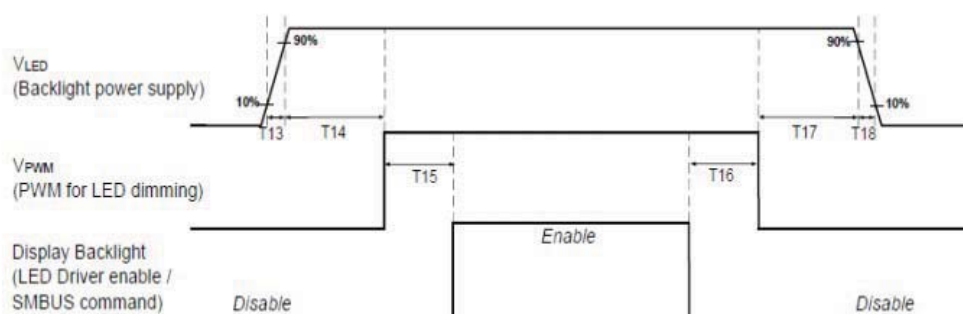
Note 4: T8 > T7



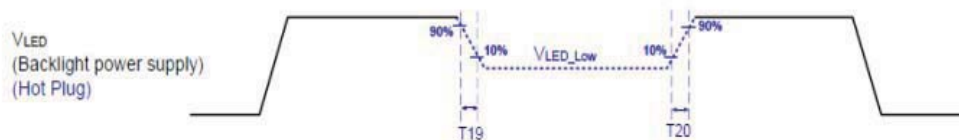
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Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

* $T_{PWM} = 1/PWM \text{ Frequency}$



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7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note I

Note I: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.

No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

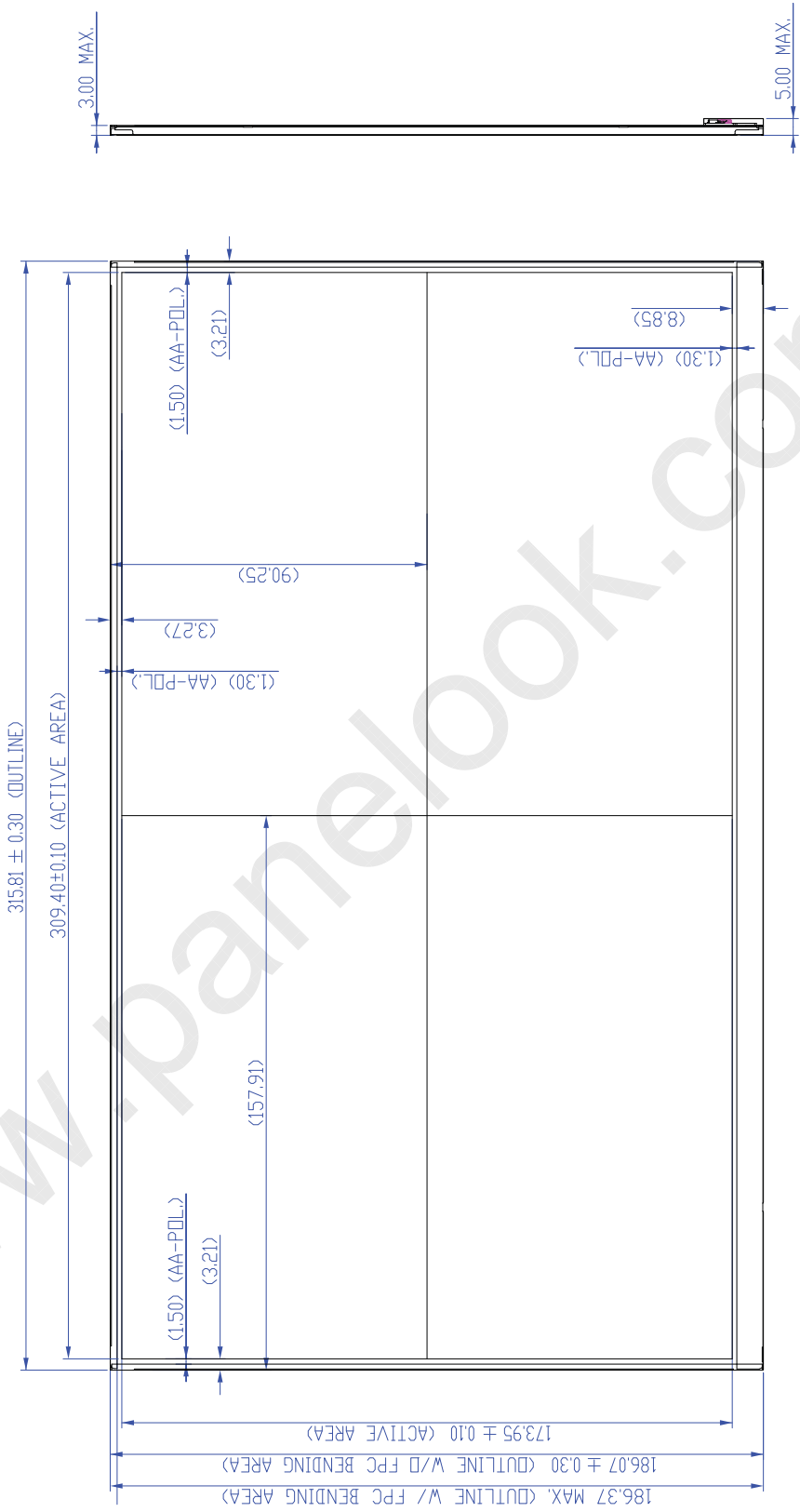


Product Specification

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8. Mechanical Characteristics

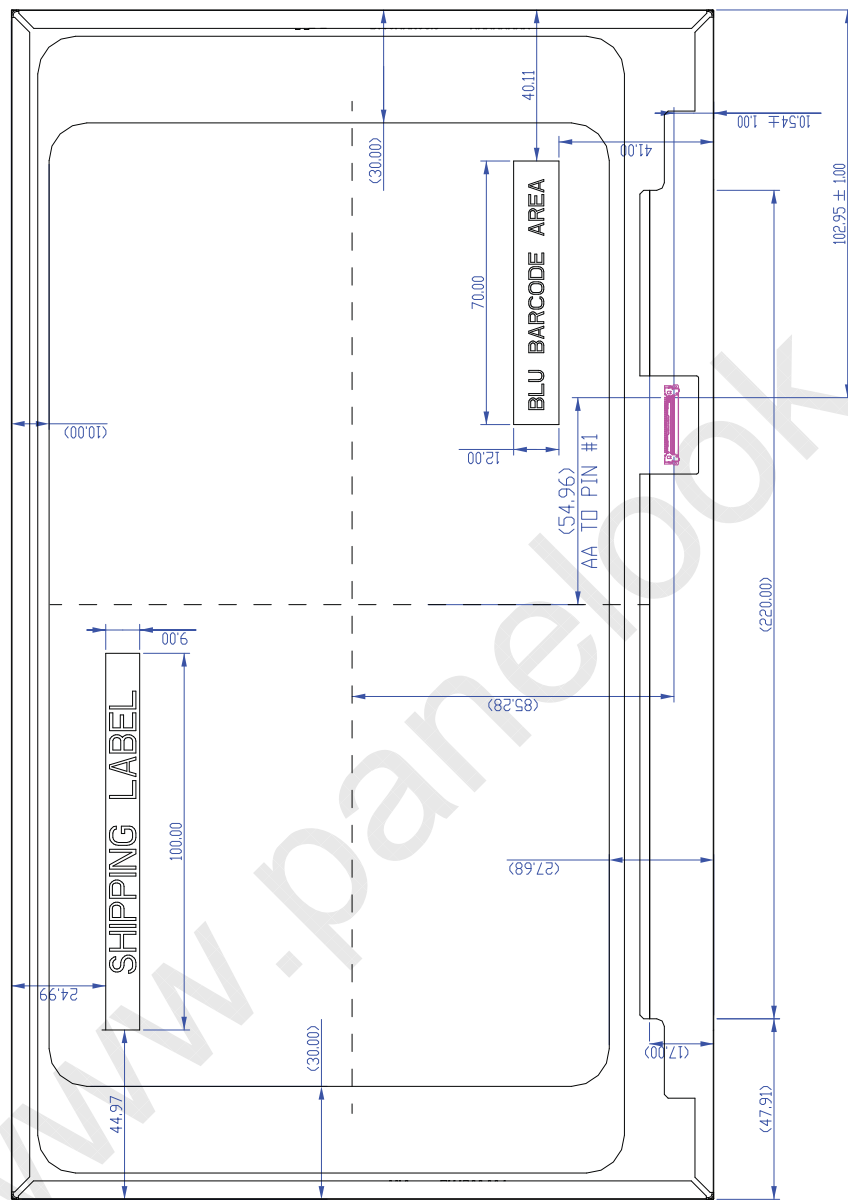
8.1 LCM Outline Dimension





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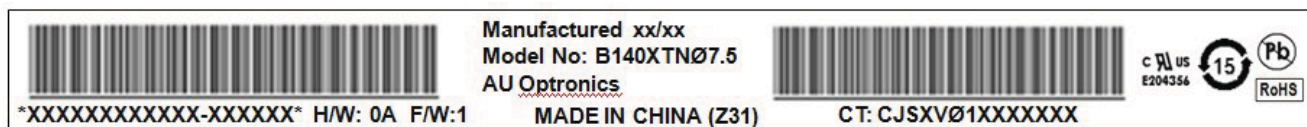


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9. Shipping and Package

9.1 Shipping Label Format

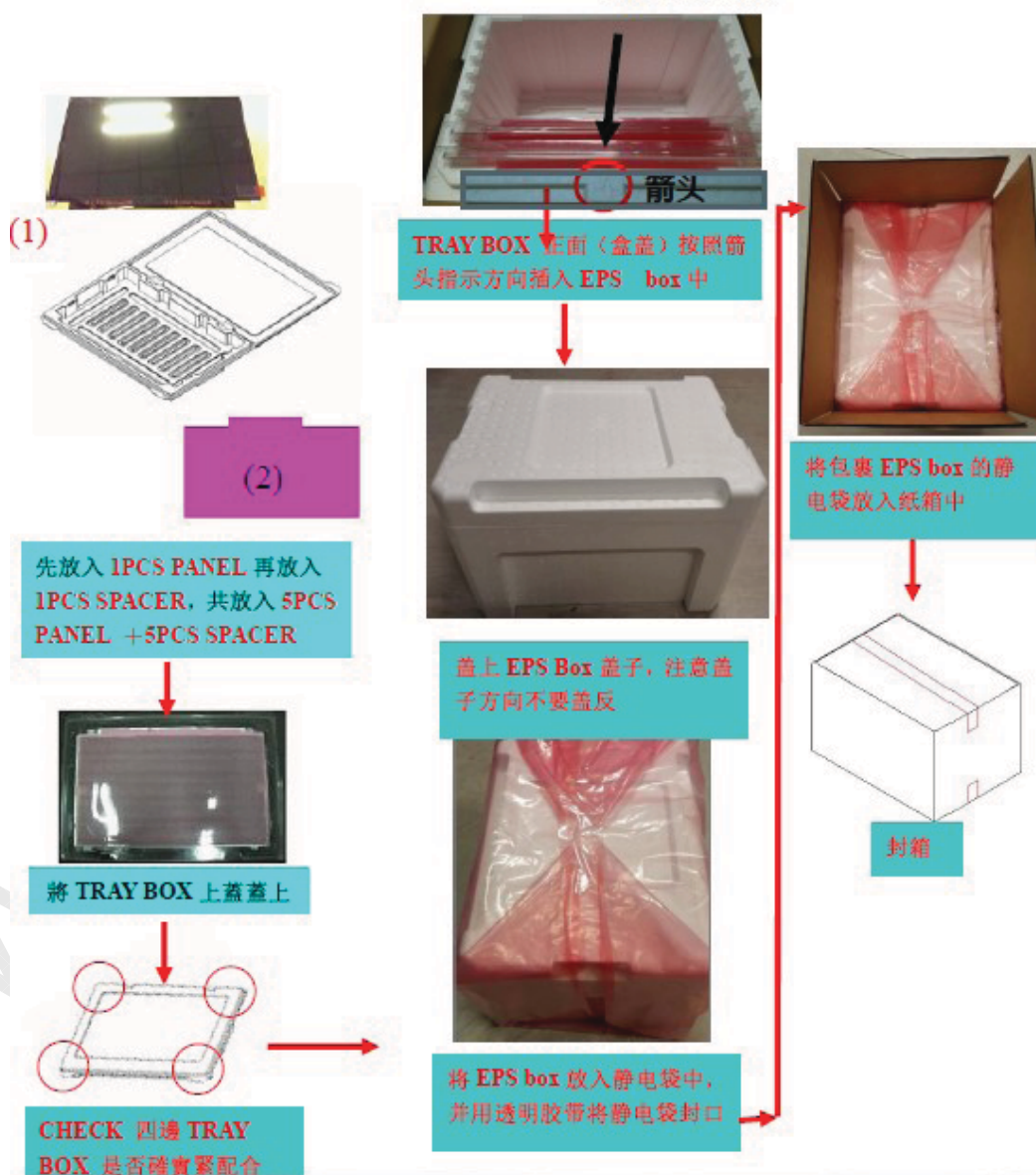


9.2 Carton Package

4.2 包裝流程圖

4.2 Packing instruction

Tray box 正面方向

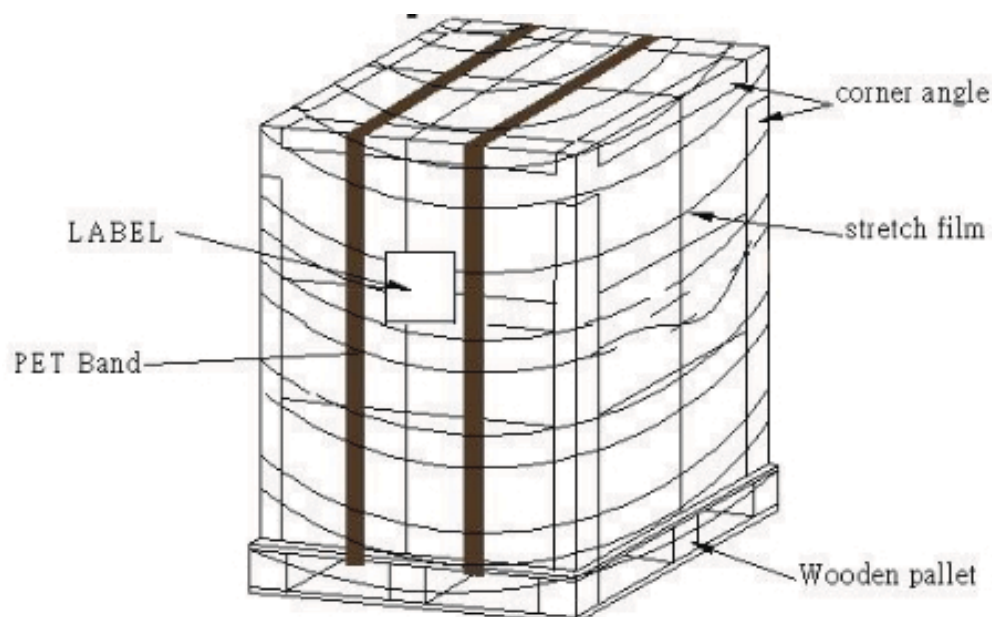




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9.3 Shipping Package of Palletizing Sequence





Product Specification

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I0. Appendix: EDID Description

I0.1 EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	90	10010000	144
0B	Product Code	02	00000010	2
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	1E	00011110	30
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	Video input def. (digital I/P, non-TMDS, CRGB)	95	10010101	149
15	Max H image size (rounded to cm)	1F	00011111	31
16	Max V image size (rounded to cm)	11	00010001	17
17	Display Gamma (=gamma*100)-100	78	01111000	120
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	03	00000011	3
19	Red/green low bits (Lower 2:2:2:2 bits)	C0	11000000	192
1A	Blue/white low bits (Lower 2:2:2:2 bits)	D5	11010101	213
1B	Red x (Upper 8 bits)	8F	10001111	143
1C	Red y/ highER 8 bits	56	01010110	86
1D	Green x	58	01011000	88
1E	Green y	93	10010011	147
1F	Blue x	29	00101001	41
20	Blue y	20	00100000	32
21	White x	50	01010000	80



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22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	CE	11001110	206
37	Pixel Clock/10000 USB	ID	00011101	29
38	Horz active Lower 8bits	56	01010110	86
39	Horz blanking Lower 8bits	E2	11100010	226
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80
3B	Vertical Active Lower 8bits	00	00000000	0
3C	Vertical Blanking Lower 8bits	1E	00011110	30
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48
3E	HorzSync. Offset	26	00100110	38
3F	HorzSync.Width	16	00010110	22
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	35	00110101	53
43	Vertical Image Size Lower 8bits	AD	10101101	173
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16
45	Horizontal Border (zero for internal LCD)	00	00000000	0
46	Vertical Border (zero for internal LCD)	00	00000000	0
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24
48	Pixel Clock/10,000 (LSB)	DF	11011111	223



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49	Pixel Clock/10,000 (MSB)	13	00010011	19
4A	Horizontal Addressable Pixels, lower 8 bits	56	01010110	86
4B	Horizontal Blanking Pixels, lower 8 bits	E2	11100010	226
4C	H Pixels, upper nibble : H Blanking, upper nibble	50	01010000	80
4D	Vertical Addressable Lines, lower 8 bits	00	00000000	0
4E	Vertical Blanking Lines, lower 8 bits	1E	00011110	30
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48
50	Horizontal Front Porch, lower 8 bits	26	00100110	38
51	Horizontal Sync Pulse, lower 8 bits	16	00010110	22
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	36	00110110	54
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0
54	Horizontal Image Size in mm, lower 8 bits	35	00110101	53
55	Vertical Image Size in mm, lower 8 bits	AD	10101101	173
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16
57	Horizontal Border	00	00000000	0
58	Vertical Border	00	00000000	0
59	Bit Encode Sync Information	18	00011000	24
5A	DC	00	00000000	0
5B	HTOTAL	00	00000000	0
5C	HA	00	00000000	0
5D	HBL	00	00000000	0
5E	HFP	00	00000000	0
5F	HFPe	00	00000000	0
60	HBP	00	00000000	0
61	HB	00	00000000	0
62	HSO	00	00000000	0
63	HS	00	00000000	0
64	VTOTAL	00	00000000	0
65	VA	00	00000000	0
66	VBL	00	00000000	0
67	VFP	00	00000000	0
68	VBP	00	00000000	0
69	VB	00	00000000	0
6A	VSO	00	00000000	0
6B	VS	00	00000000	0
6C	Detail Timing Description #4	00	00000000	0
6D	Flag	00	00000000	0



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6E	Reserved	00	00000000	0
6F	For Brightness Table and Power Consumption	02	00000010	2
70	Flag	00	00000000	0
71	PWM % [7:0] @ Step 0	10	00010000	16
72	PWM % [7:0] @ Step 5	48	01001000	72
73	PWM % [7:0] @ Step 10	FF	11111111	255
74	Nits [7:0] @ Step 0	0F	00001111	15
75	Nits [7:0] @ Step 5	3C	00111100	60
76	Nits [7:0] @ Step 10	7D	01111101	125
77	Panel Electronics Power @ 32x32 Chess Pattern =	48	01001000	72
78	Backlight Power @ 60 nits =	0F	00001111	15
79	Backlight Power @ Step 10 =	1B	00011011	27
7A	Nits [7:0] @ 100% PWM Duty =	7D	01111101	125
7B	Flag	20	00100000	32
7C	Flag	20	00100000	32
7D	Flag	20	00100000	32
7E	Extension Flag	00	00000000	0
7F	Checksum	09	00001001	9

I0.2 Notes

DPCD Ver.	sDRRS	DCR	DMRRS	PSR	MBO	VESA DSC	MSO	Free-Sync	HDR	Dimming
1.2	on	N/A	N/A	N/A	N/A	off	N/A	on	N/A	N/A